WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type provided on the first semiconductor layer;

a trench penetrating the second semiconductor layer and intruding into the first semiconductor layer;

a thick gate insulating film provided on a inner wall of the trench below an upper surface of the first semiconductor layer;

a thin gate insulating film provided on the inner wall of the trench at a part upper than the thick gate insulating film;

a gate electrode filling the trench; and

a semiconductor region of a second conductivity type selectively formed to adjoin the trench and to project from a bottom surface of the second semiconductor layer into the first semiconductor layer.

2. The semiconductor device according to claim 1, wherein:

a lower end of a part of the semiconductor region of the second conductivity type in contact with the trench is substantially at a same level as a boundary between the thick gate insulating film and the thin gate insulating film.

3. The semiconductor device according to claim 1, wherein:

a carrier concentration of the semiconductor region of the second conductivity type is higher than a carrier concentration of the first semiconductor layer and lower than a carrier concentration of the second semiconductor

layer.

4. The semiconductor device according to claim 1, wherein:

the thick gate insulating film has a thickness smaller than a half of a width of the trench,

a recess enclosed by the thick gate insulating film is provided near a bottom of the trench, and

the gate electrode fills the recess.

5. The semiconductor device according to claim 1, wherein:

a bottom of the trench is filled with the thick gate insulating film so that a flat surface is formed by the thick gate insulating film.

6. The semiconductor device according to claim 1, wherein:

the semiconductor region of the second conductivity type is formed in a self-aligning fashion to the thick gate insulating film.

7. The semiconductor device according to claim 1, wherein:

a channel is able to be formed near the trench in a part of the second semiconductor layer and in a part of the semiconductor region by applying a predetermined voltage to the gate electrode.

8. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type provided on the first semiconductor layer;

a trench penetrating the second semiconductor layer

and intruding into the first semiconductor layer;

a thick gate insulating film provided on a inner wall of the trench below an upper surface of the first semiconductor layer;

a thin gate insulating film provided on the inner wall of the trench at a part upper than the thick gate insulating film;

a gate electrode filling the trench; and

a semiconductor region of a second conductivity type adjoining the trench, the semiconductor region being formed by selectively reversing the conductivity type of a part of the first semiconductor layer near the second semiconductor layer.

9. The semiconductor device according to claim 8, wherein:

a lower end of a part of the semiconductor region of the second conductivity type in contact with the trench is substantially at a same level as a boundary between the thick gate insulating film and the thin gate insulating film.

10. The semiconductor device according to claim 8, wherein:

a carrier concentration of the semiconductor region of the second conductivity type is higher than a carrier concentration of the first semiconductor layer and lower than a carrier concentration of the second semiconductor layer.

11. The semiconductor device according to claim 8, wherein:

the thick gate insulating film has a thickness smaller than a half of a width of the trench,

a recess enclosed by the thick gate insulating film is provided near a bottom of the trench, and

the gate electrode fills the recess.

12. The semiconductor device according to claim 8, wherein:

a bottom of the trench is filled with the thick gate insulating film so that a flat surface is formed by the thick gate insulating film.

13. The semiconductor device according to claim 8, wherein:

the semiconductor region of the second conductivity type is formed in a self-aligning fashion to the thick gate insulating film.

14. The semiconductor device according to claim 8, wherein:

a channel is able to be formed near the trench in a part of the second semiconductor layer and in a part of the semiconductor region by applying a predetermined voltage to the gate electrode.

15. A method to manufacture a semiconductor device comprising:

forming a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type provided on the first semiconductor layer, a trench penetrating the second semiconductor layer and intruding into the first semiconductor layer, and a thick gate insulating film provided on a inner wall of the trench below an upper surface of the first semiconductor layer;

introducing an impurity of a second conductivity type into a part of the first semiconductor layer above the thick gate insulating film and adjoining the trench to form a semiconductor region of a second conductivity type;

forming a thin gate insulating film on the inner wall of the trench at a part upper than the thick gate insulating film; and

filling the trench with a gate electrode.

16. The method to manufacture a semiconductor device according to claim 15 wherein:

the semiconductor region of the second conductivity type is formed by introducing the impurity of the second conductivity type from an inner wall of the trench by using the thick gate insulating film as a mask.

17. The method to manufacture a semiconductor device according to claim 15 wherein:

the semiconductor region of the second conductivity type is formed by implanting the impurity of the second conductivity type from a surface of the second semiconductor layer.

18. The method to manufacture a semiconductor device according to claim 15 wherein:

the forming the thin gate insulating film is performed before the introducing the impurity of the second conductivity type, and

the impurity of the second conductivity type is introduced through the thin gate insulating film into the part of the first semiconductor layer.

19. The method to manufacture a semiconductor device according to claim 15 wherein:

a lower end of a part of the semiconductor region of the second conductivity type in contact with the trench is substantially at a same level as a boundary between the thick gate insulating film and the thin gate insulating film.

20. The method to manufacture a semiconductor device according to claim 15 wherein:

a carrier concentration of the semiconductor region of the second conductivity type is higher than a carrier concentration of the first semiconductor layer and lower than a carrier concentration of the second semiconductor layer.